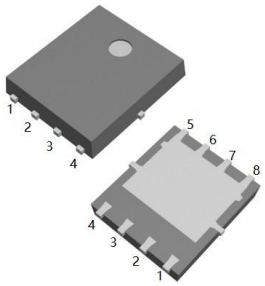
# D50N04EL

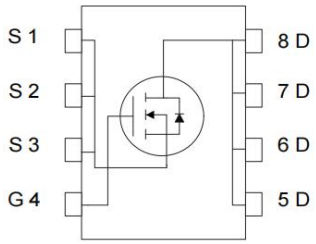
## 50 Amps,40Volts N-CHANNEL Power MOSFET

### FEATURE

- 50A,40V,$R_{DS(ON)MAX}$=10mΩ $V_{GS}$=10V/1A
  $R_{DS(ON)MAX}$=12mΩ @$V_{GS}$=4.5V/1A
- Low gate charge
- Low $C_{iss}$
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability

**DFN5*6**




## Absolute Maximum Ratings($T_C$=25℃,unless otherwise noted)

| Parameter | Symbol | D50N04EL | UNIT |
|---|---|---|---|
| Drain-Source Voltage | $V_{DSS}$ | 40 | V |
| Gate-Source Voltage | $V_{GS}$ | ±20 | |
| Continuous Drain Current | $I_D$ | 50 | A |
| Pulsed Drain Current(Note1) | $I_{DM}$ | 200 | |
| Single Pulse Avalanche Energy (Note 2) | $E_{AS}$ | 72 | mJ |
| Operating Junction and Storage Temperature Range | $T_J$,$T_{STG}$ | -55 to +150 | ℃ |
| Maximum lead temperature for soldering purposes, 1/8″from case for 5 seconds | $T_L$ | 260 | ℃ |

## Thermal Characteristics

| Parameter | | Symbol | MAX | Units |
|---|---|---|---|---|
| Thermal resistance , Channel to Case | | $R_{th(ch-c)}$ | 3.57 | ℃/W |
| Maximum Power Dissipation | $T_C$=25℃ | $P_D$ | 35 | W |

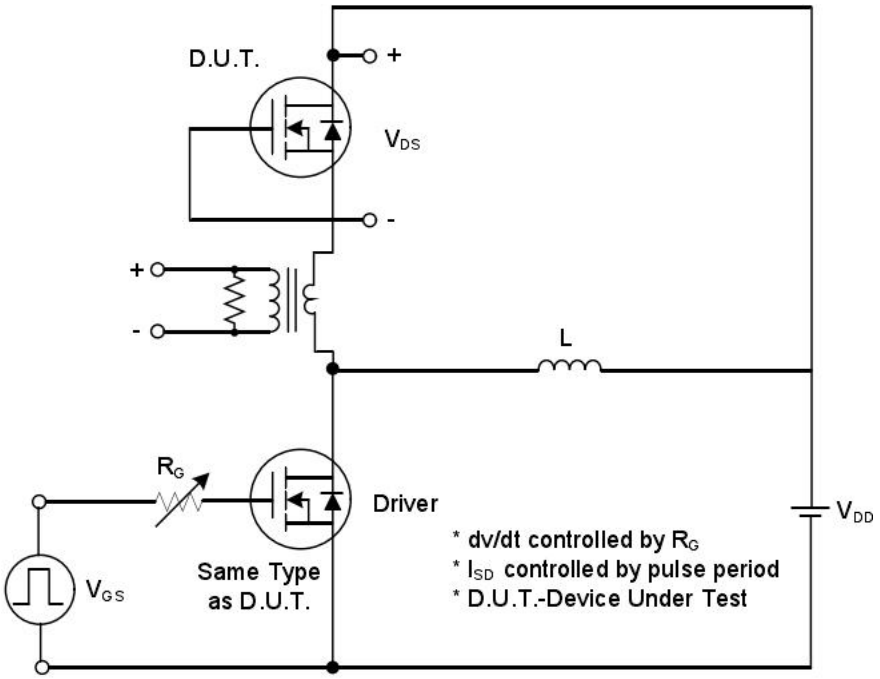
## Electrical Characteristics ($T_c$=25℃,unless otherwise noted)

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Off Characteristics** | | | | | | |
| Drain-Source Breakdown Voltage | $BV_{DSS}$ | $V_{GS}$=0V,$I_D$=250uA | 40 | — | — | V |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$=40$V_{GS}$=0V | — | — | 1 | μA |
| Gate-Body Leakage Current,Forward | $I_{GSSF}$ | $V_{GS}$=20V,$V_{DS}$=0V | — | — | 100 | nA |
| Gate-Body Leakage Current,Reverse | $I_{GSSR}$ | $V_{GS}$=-20V,$V_{DS}$=0V | — | — | -100 | nA |
| **On Characteristics** | | | | | | |
| Gate-Source Threshold Voltage | $V_{GS(th)}$ | $V_{DS}$=$V_{GS}$,$I_D$=250uA | 1.0 | — | 2.5 | V |
| Drain-Source On-State Resistance | $R_{DS(on)}$ | $V_{GS}$=10V,$I_D$=1A | — | 8.5 | 10 | mΩ |
| | $R_{DS(on)}$ | $V_{GS}$=4.5V,$I_D$=1A | — | 10 | 12 | mΩ |
| **Dynamic Characteristics** | | | | | | |
| Input Capacitance | $C_{iss}$ | $V_{DS}$=25V,$V_{GS}$=0V, f=1.0MHZ | — | 1330 | — | pF |
| Output Capacitance | $C_{oss}$ | | — | 109 | — | pF |
| Reverse Transfer Capacitance | $C_{rss}$ | | — | 98 | — | pF |
| **Switching Characteristics** | | | | | | |
| Turn-On Delay Time | $t_{d(on)}$ | $V_{DS}$=20V,$R_G$=10Ω $I_D$=12A,$V_{GS}$=10V | — | 0.6 | — | ns |
| Turn-On Rise Time | $t_r$ | | — | 12.4 | — | ns |
| Turn-Off Delay Time | $t_{d(off)}$ | | — | 46.4 | — | ns |
| Turn-Off Fall Time | $t_f$ | | — | 14.2 | — | ns |
| Total Gate Charge | Qg | $V_{DS}$=32V,$I_D$=12A, $V_{GS}$=10V | — | 33 | — | nC |
| Gate-Source Charge | Qgs | | — | 10.8 | — | nC |
| Gate-Drain Charge | Qgd | | — | 4.2 | — | nC |
| **Drain-Source Body Diode Characteristics and Maximum Ratings** | | | | | | |
| Diode Forward Voltage | $V_{SD}$ | $I_S$=1A,$V_{GS}$=0V | — | — | 1.2 | V |
| Reverse Recovery Time | $t_{rr}$ | Vdd=30V,$I_F$=1A, dI$_F$/dt=100A/us，(Note3) | — | 14 | — | ns |
| Reverse Recovery Charge | Qrr | | — | 6 | — | nC |

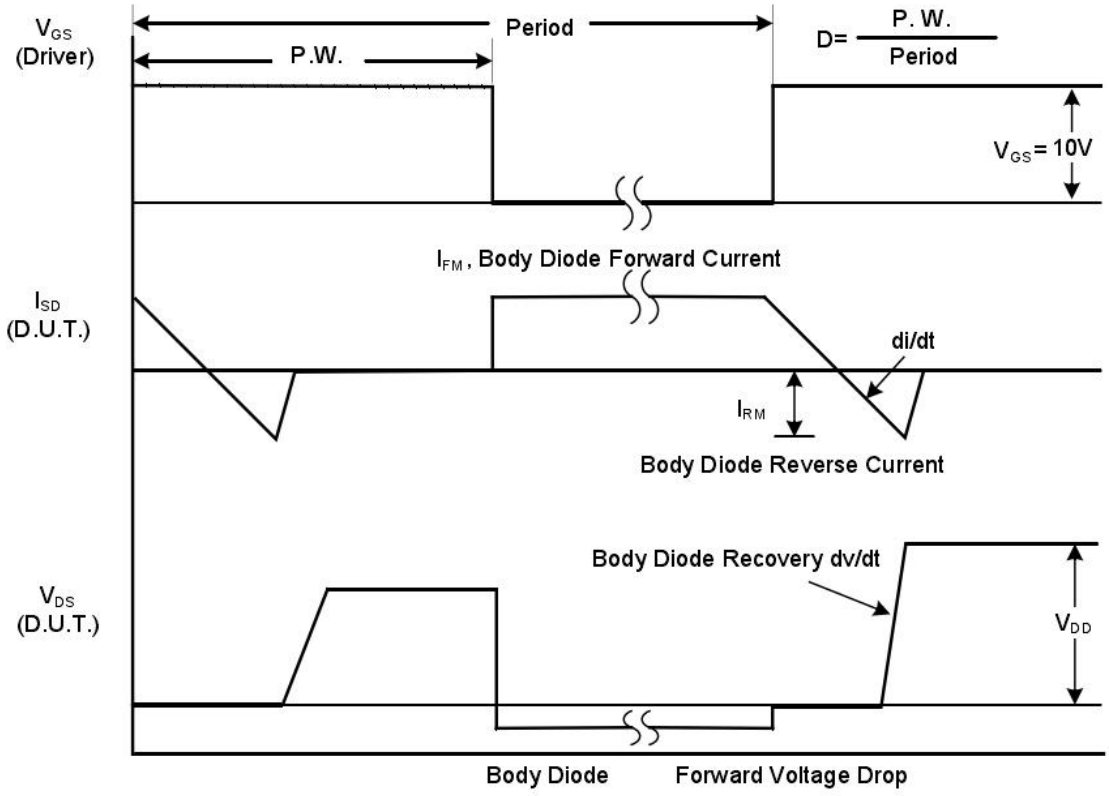
**Notes**

1. Repetitive Rating:pulse width limited by maximum junction temperature.
2. L=0.5mH,$R_g$=25Ω,$V_{DD}$=32V ,starting $T_J$=25℃.
3. Pulse width≤300us;duty cycle≤2%.

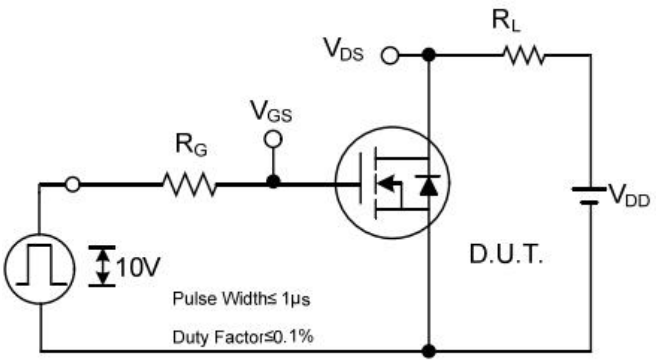
## RATINGAND CHARACTERISTIC CURVES



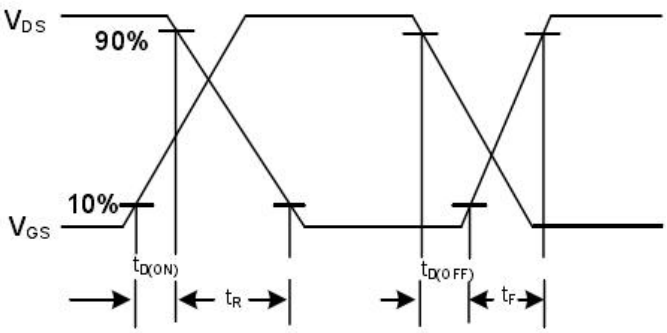

**Peak Diode Recovery dv/dt Test Circuit**



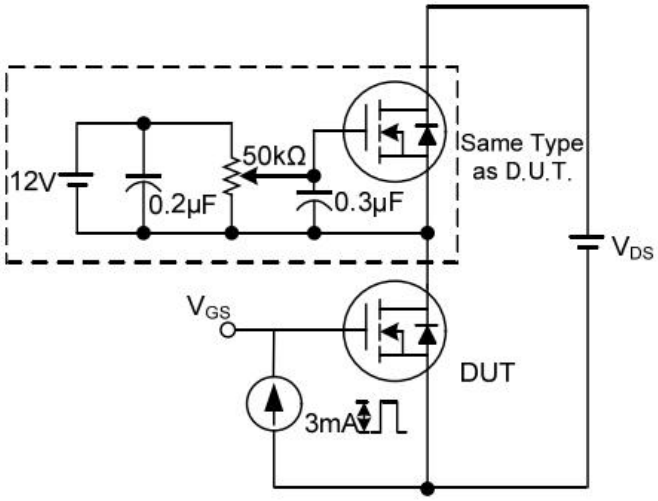

**Peak Diode Recovery dv/dt Waveforms**



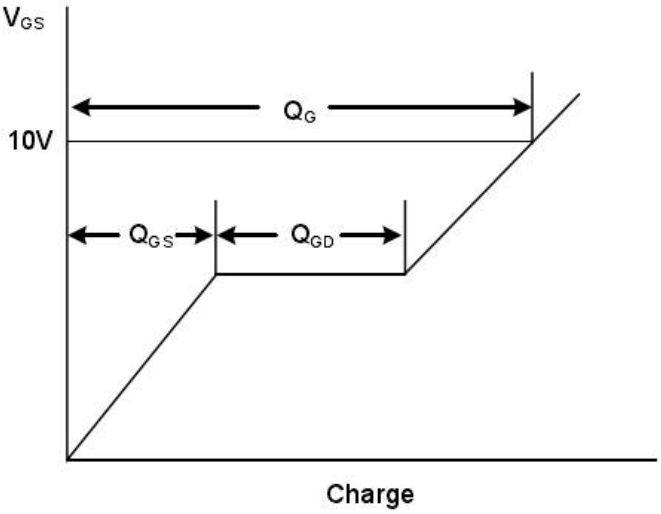

**Switching Test Circuit**



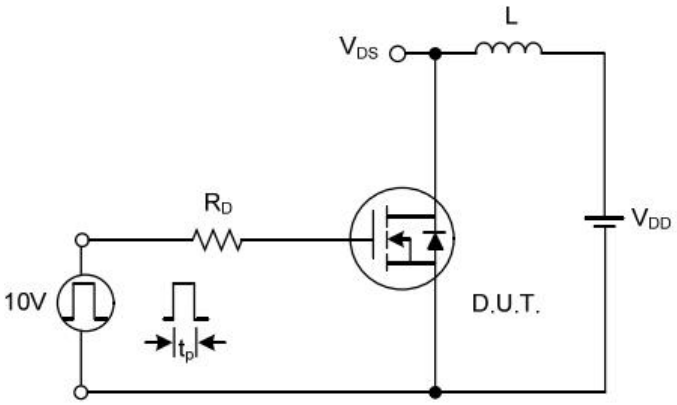

**Switching Waveforms**



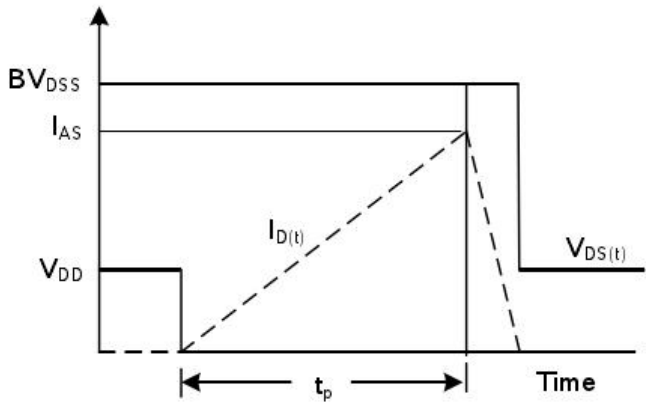

**Gate Charge Test Circuit**




**Gate Charge Waveform**




**Unclamped Inductive Switching Test Circuit**




**Unclamped Inductive Switching Waveforms**

## RATINGAND CHARACTERISTIC CURVES

Figure.1 Typical Output Characteristics

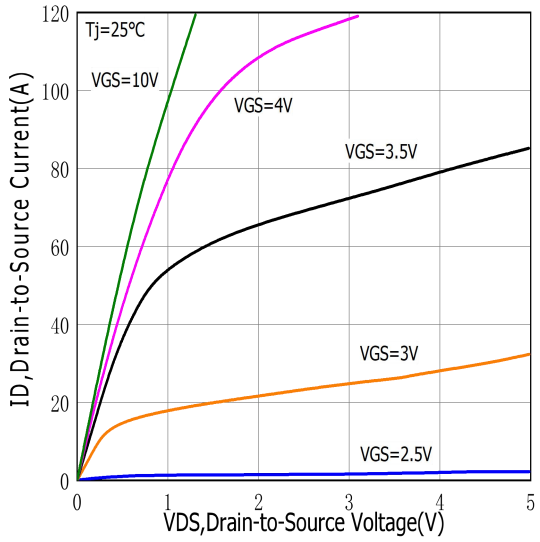



Figure.2 Typical Gate Charge vs Gate to Source Voltage

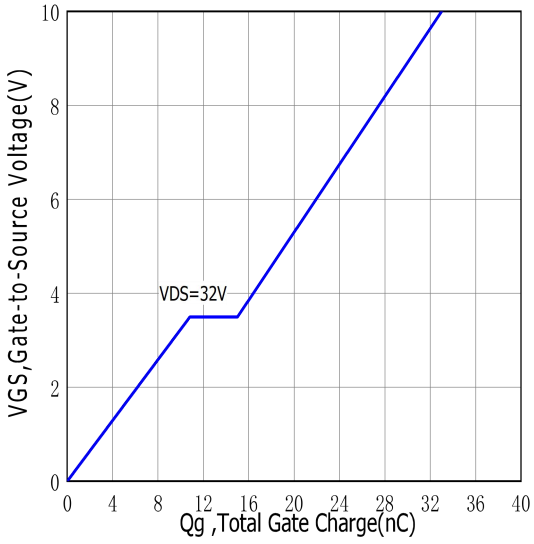



Figure.3 Typical Body Diode Transfer Characteristics

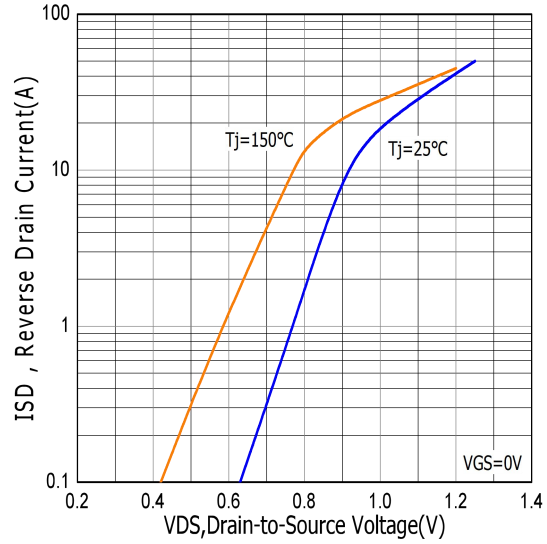



Figure.4 Typical Capacitance vs Drain to Source Voltage

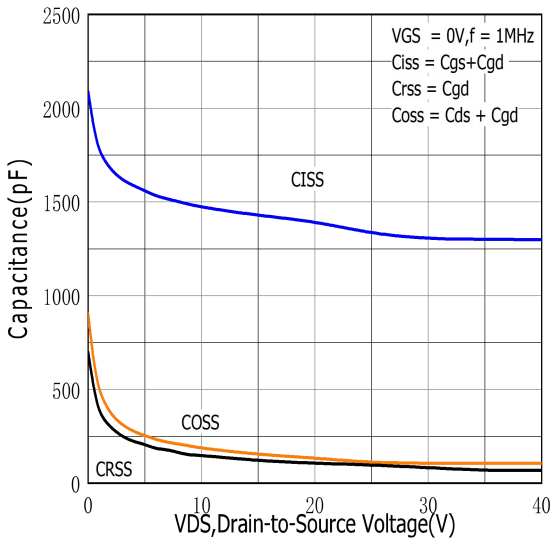



Figure.5 Typical Breakdown Voltage vs Junction Temperature

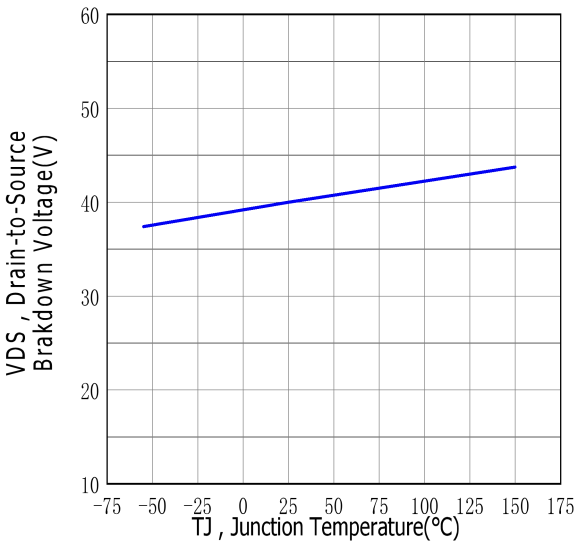



Figure.6 Typical Drian to Source on Resistance vs Junction Temperature

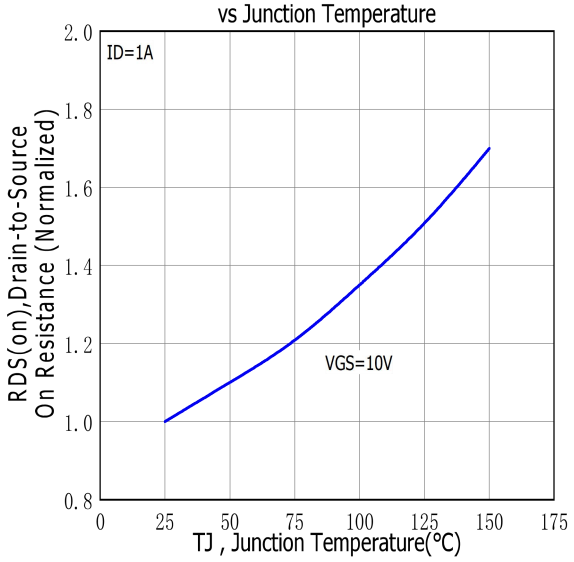


Figure.7 Maximum Forward Bias Safe Operating Area

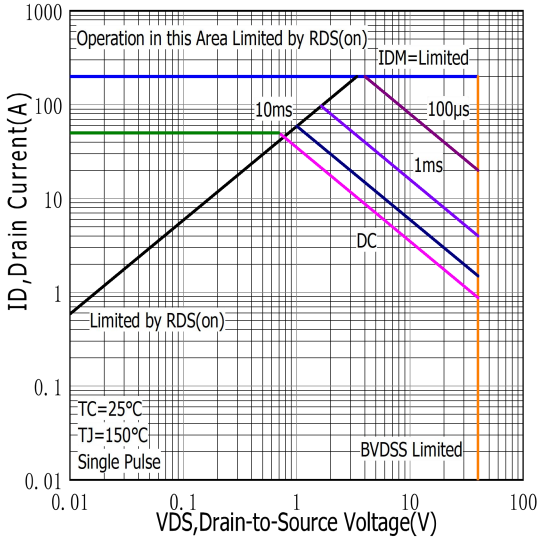



Figure.8 Typical Drain to Source ON Resistance vs Drain Current

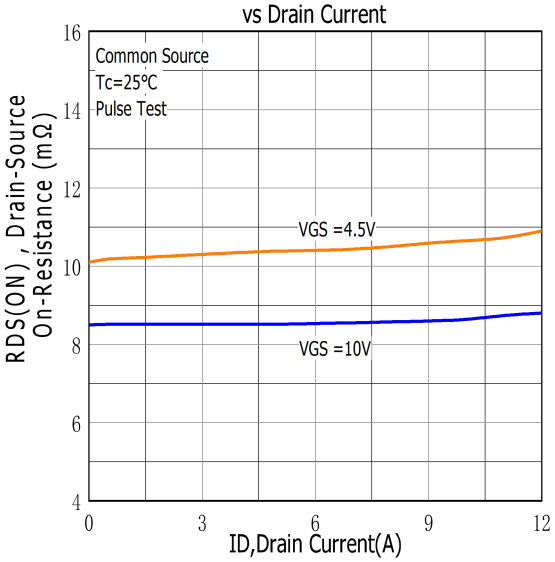



Figure.9 Maximum EAS vs Channel Temperature

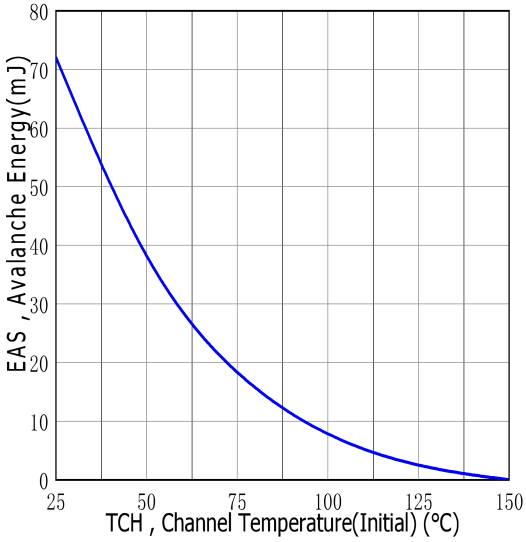



Figure.10 Typical Threshold Voltage vs Case Temperature

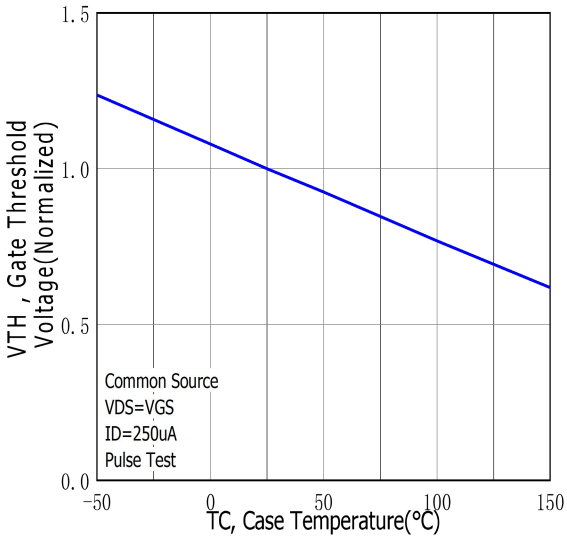



Figure.11 Maximum Effective Thermal Impedance , Junction to Case

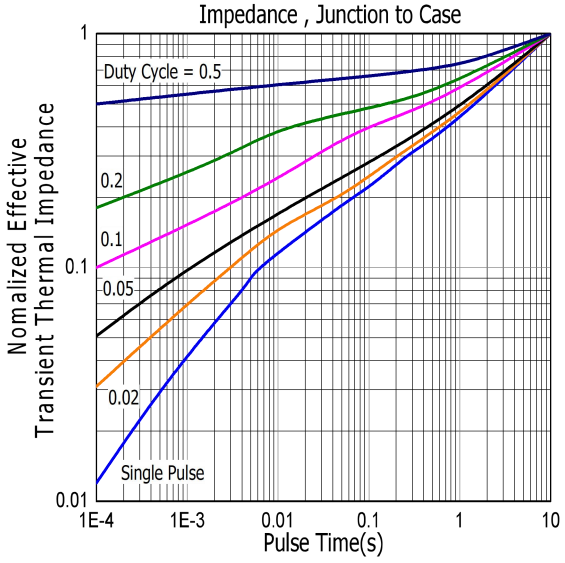
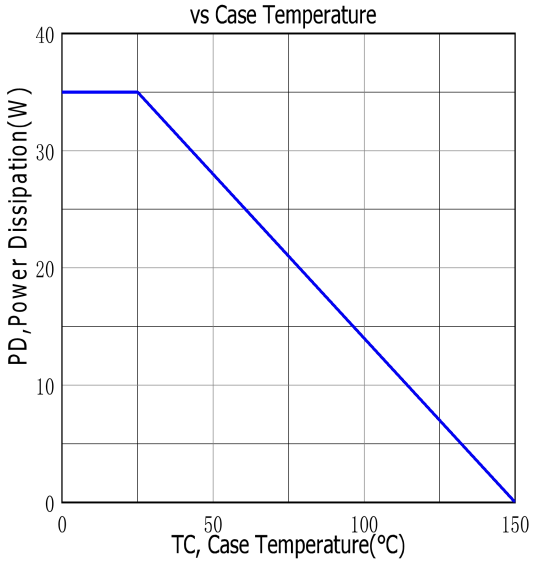



Figure.12 Maximum Power Dissipation vs Case Temperature



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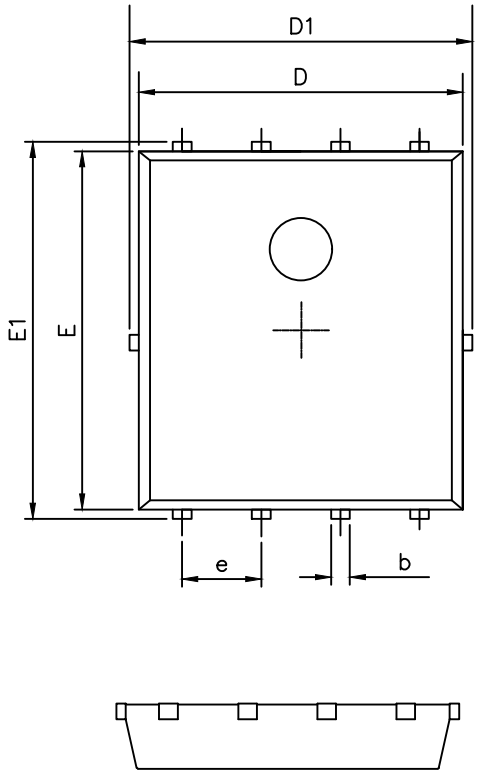
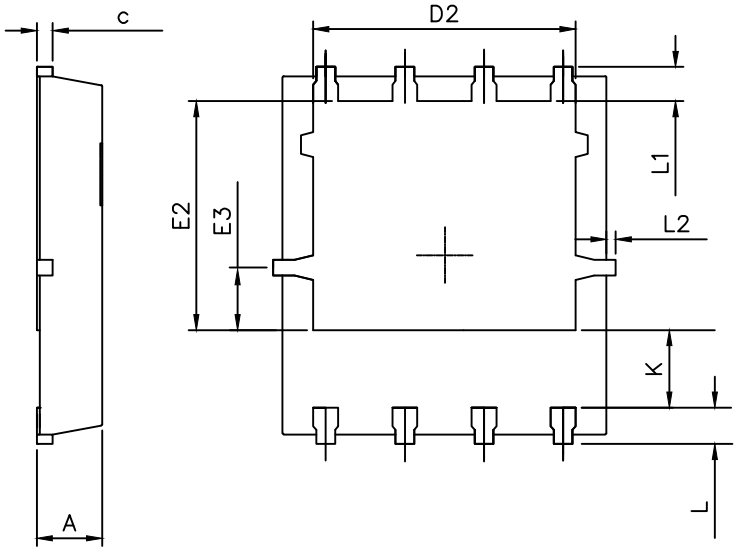
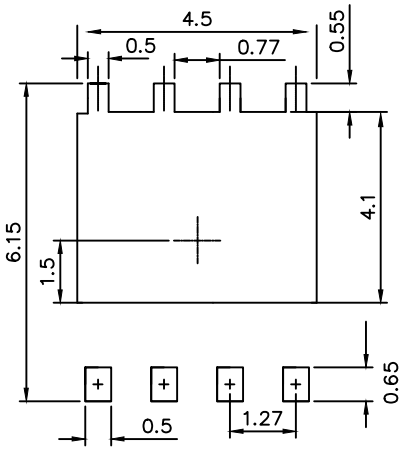
CHONGQING PINGWEI ENTERPRISE CO.,LTD

# DFN5x6 PACKAGE OUTLINE




RECOMMENDED LAND PATTERN




UNIT: mm

| | MIN | NOM | MAX |
|---|---|---|---|
| A | 0.90 | 1.00 | 1.10 |
| b | 0.25 | 0.35 | 0.50 |
| c | 0.10 | 0.20 | 0.30 |
| D | 4.80 | 5.00 | 5.30 |
| D1 | 4.90 | 5.10 | 5.50 |
| D2 | 3.92 | 4.02 | 4.20 |
| E | 5.65 | 5.75 | 5.85 |
| E1 | 5.90 | 6.05 | 6.20 |
| E2 | 3.325 | 3.525 | 3.775 |
| E3 | 0.80 | 0.90 | 1.00 |
| e | | 1.27 | |
| L | 0.40 | 0.55 | 0.70 |
| L1 | | 0.65 | |
| L2 | 0.00 | | 0.15 |
| K | 1.00 | 1.30 | 1.50 |